CLAIMS

We I claim:

1. A method for fabricating at least one mesa or ridge structure in a layer or layer sequence, in which sidewalls of the mesa or ridge structure are provided with a coating applied after the uncovering thereof, having the following method steps:

a) application of a sacrificial layer above the layer or layer sequence;

b) application and patterning of a mask layer above the sacrificial layer for definition of the mesa or ridge dimensions;

c) partial removal of the sacrificial layer and of the layer or layer sequence, to form the mesa or ridge structure in the layer or layer sequence;

d) selective removal of a part of the sacrificial layer from the side areas thereof which have been uncovered in step c), so that a sacrificial layer remains which is narrower in comparison with a layer that has remained above the sacrificial layer as seen from the layer or layer sequence;

e) application of the coating at least to the sidewalls of the structure produced in steps a) to d) so that the side areas of the residual sacrificial layer are not completely overformed by the coating material; and

f) at least partial removal of the sacrificial layer, so that the layer that has remained above the sacrificial layer as seen from the layer or layer sequence is lifted off.

2. The method as claimed in claim 1, in which, in step f), the sacrificial layer is removed completely, to produce a window toward the layer or layer sequence in the coating.

3. The method as claimed in claim 2, in which an electrical connection metallization is applied to the layer or layer sequence in the window.

4. A method for fabricating at least one ridge waveguide laser diode chip based on $In_xAl_yGa_{1-x-y}N$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x+y \leq 1$, in which the geometrical ridge waveguide structure is fabricated by means of a method as claimed in claim 1.

5. The method as claimed in claim 4, in which the width of the ridge waveguide structure is less than or equal to 2 μm.

6. The method as claimed in claim 4, in which, in step c), the facets of the laser diode chip are produced by means of dry etching and the coating contains a reflective or antireflective layer system.

7. A method for fabricating at least one light-emitting diode chip with coating of the side areas of the radiation-generating layer sequence, in which the geometrical structure of the radiation-generating layer sequence and the coating are produced by means of a method as claimed in claim 1.

8. The method as claimed in claim 7, in which an edge length of the light-emitting diode chip is less than or equal to 2 µm.

9. A method for fabricating at least one gain-controlled laser diode in a layer sequence, in particular based on $In_xAl_yGa_{1-x-y}N$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x+y \leq 1$, having the following method steps:

a) application of a sacrificial layer above the layer sequence;

b) application and patterning of a mask layer above the sacrificial layer;

c) partial removal of the sacrificial layer in the regions not covered by the mask layer;

d) selective removal of a part of the sacrificial layer from the side areas thereof which have been uncovered in step c), so that a sacrificial layer remains which is narrower in comparison with a layer that has remained above the sacrificial layer as seen from the layer sequence, which narrower sacrificial layer defines the electrically pumped region of the laser diode;

e) application of a coating at least to the sidewalls of the structure produced in steps a) to d) so that the side areas of the residual sacrificial layer are not completely overformed by the coating material; and

f) at least partial removal of the sacrificial layer, so that the layer that has remained above the sacrificial layer as seen from the layer or layer sequence is lifted off.

10. The method as claimed in claim 9, in which the width of the pumped region is less than or equal to 2 µm.

11. The method as claimed in claim 9, in which, in step f), the sacrificial layer is removed completely, so that a window toward the layer sequence is produced in the coating.

12. The method as claimed in claim 11, in which an electrical connection metallization is applied to the layer sequence in the window.

13. The method as claimed in claim 9, in which the sacrificial layer comprises a metal, a dielectric, a polymer, an epitaxially grown material or a combination of these materials.

14. The method as claimed in claim 9, in which step b) effects the application and patterning of a first mask layer above the sacrificial layer and a second mask layer above the first mask layer.

15. The method as claimed in claim 9, in which a covering layer is applied before the application of the mask layer above the sacrificial layer.

16. The method as claimed in claim 10, in which the width of the ridge waveguide structure, the edge length or, respectively, the width of the pumped region is less than or equal to 1.5 µm.

17. The method as claimed in claim 1, in which the sacrificial layer comprises a metal, a dielectric, a polymer, an epitaxially grown material or a combination of these materials.

18. The method as claimed in claim 1, in which step b) effects the application and patterning of a first mask layer above the sacrificial layer and a second mask layer above the first mask layer.

19. The method as claimed in claim 1, in which a covering layer is applied before the application of the mask layer above the sacrificial layer.

20. The method as claimed in claim 4, in which the width of the ridge waveguide structure, the edge length or, respectively, the width of the pumped region is less than or equal to 1.5 µm.

21. The method as claimed in claim 8, in which the width of the ridge waveguide structure, the edge length or, respectively, the width of the pumped region is less than or equal to 1.5 µm.

22. The method of claim 1, wherein said partial removal of the sacrificial layer is done by anisotropic etching.

23. The method of claim 9, wherein said partial removal of the sacrificial layer is done by anisotropic etching.